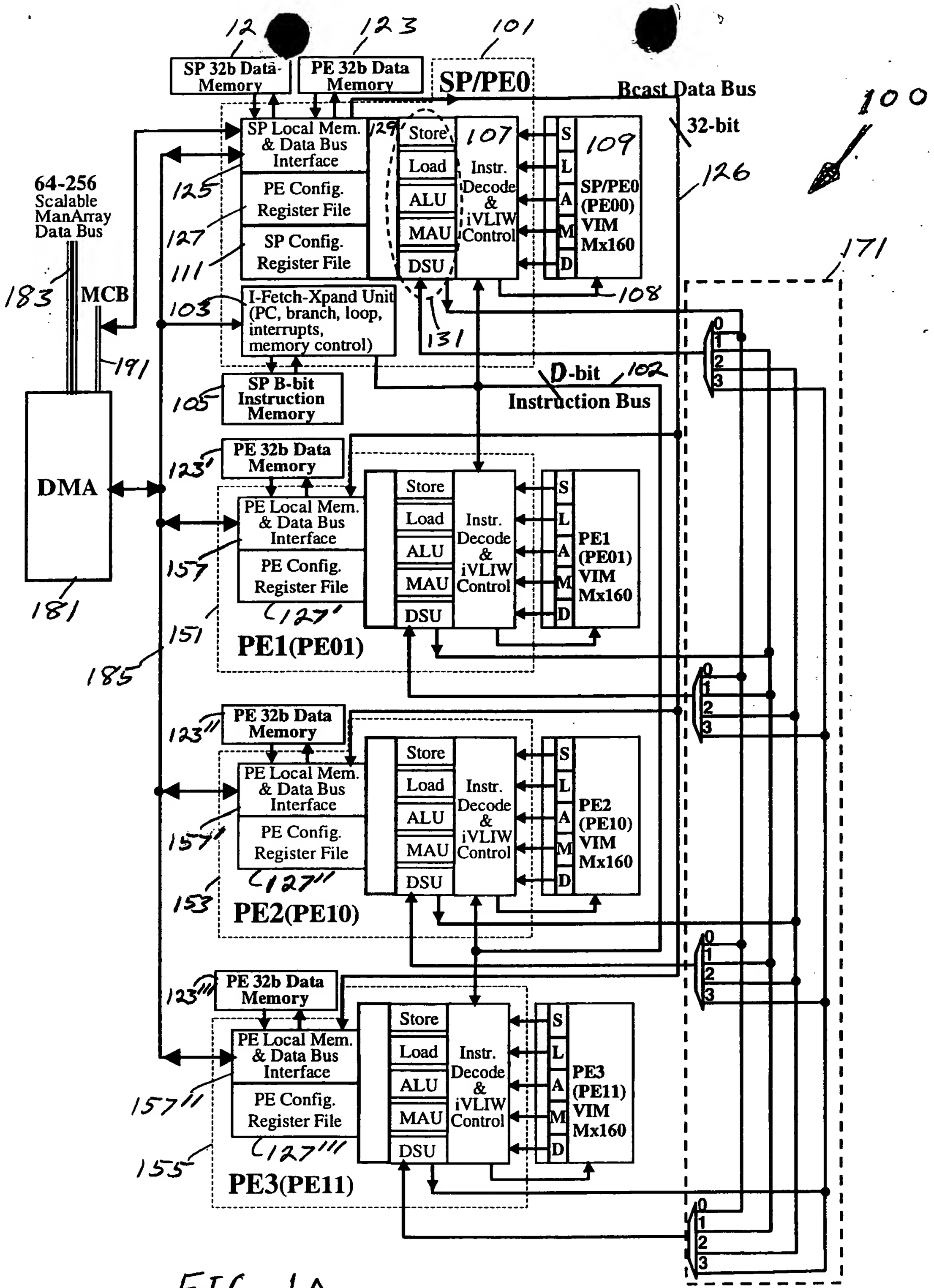
12
123
101
SP 32b Data Memory
PE 32b Data Memory
SP/PE0
Bcast Data Bus
32-bit
100
126
SP Local Mem. & Data Bus Interface
129
Store
Load
ALU
MAU
DSU
107
Instr. Decode & iVLIW Control
S
L
A
M
D
109
SP/PE0 (PE00) VIM Mx160
125
PE Config. Register File
127
SP Config. Register File
111
64-256 Scalable ManArray Data Bus
183
MCB
191
I-Fetch-Xpand Unit (PC, branch, loop, interrupts, memory control)
103
108
131
171
0
1
2
3
D-bit
102
Instruction Bus
SP B-bit Instruction Memory
105
DMA
181
PE 32b Data Memory
123'
PE Local Mem. & Data Bus Interface
157
PE Config. Register File
127'
PE1(PE01)
151
185
PE1 (PE01) VIM Mx160
PE 32b Data Memory
123''
PE Local Mem. & Data Bus Interface
157''
PE Config. Register File
127''
153
PE2(PE10)
PE2 (PE10) VIM Mx160
PE 32b Data Memory
123'''
PE Local Mem. & Data Bus Interface
157'''
PE Config. Register File
127'''
155
PE3(PE11)
PE3 (PE11) VIM Mx160

FIG. 1A

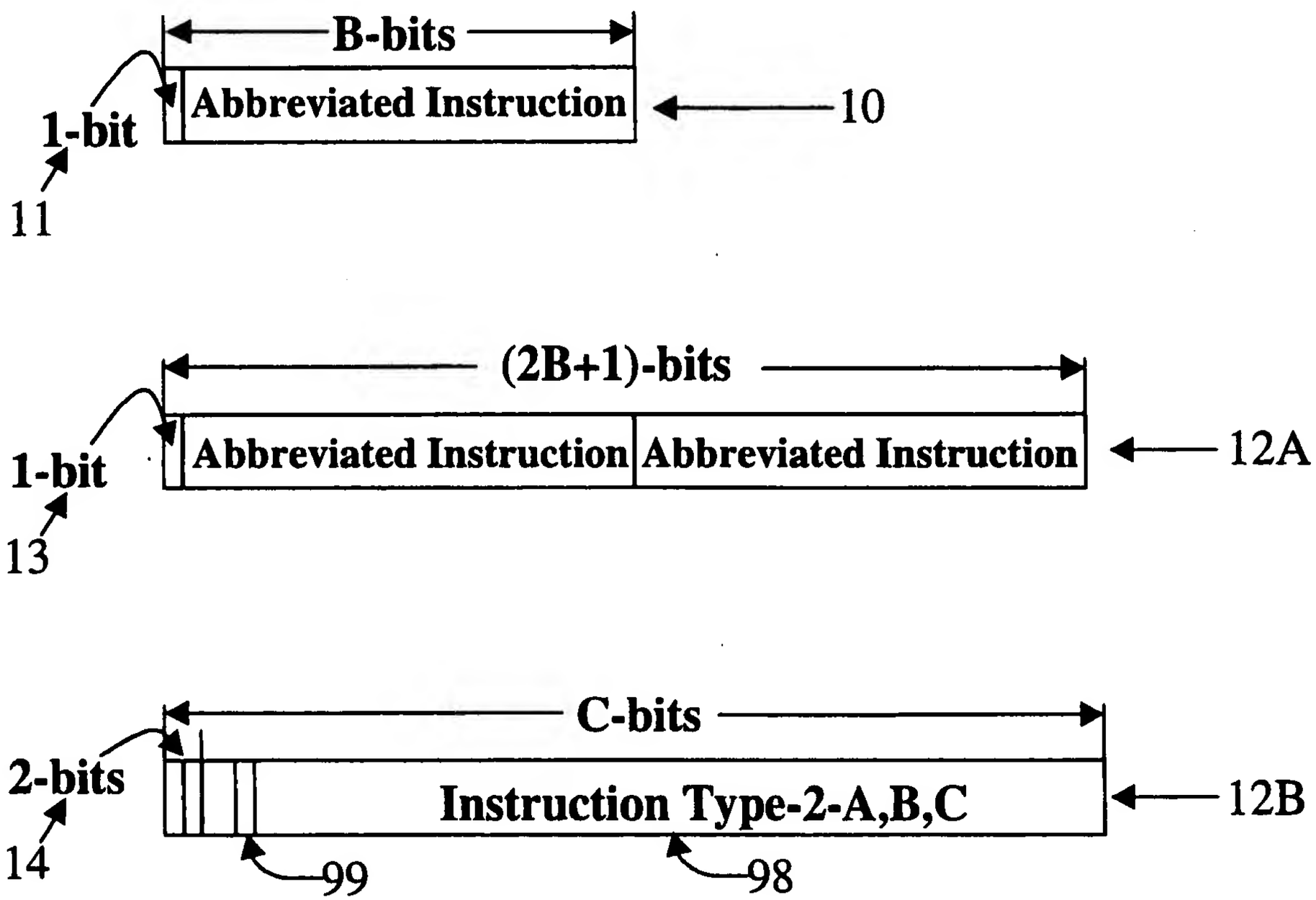

FIG. 1B

09420115 - 102109

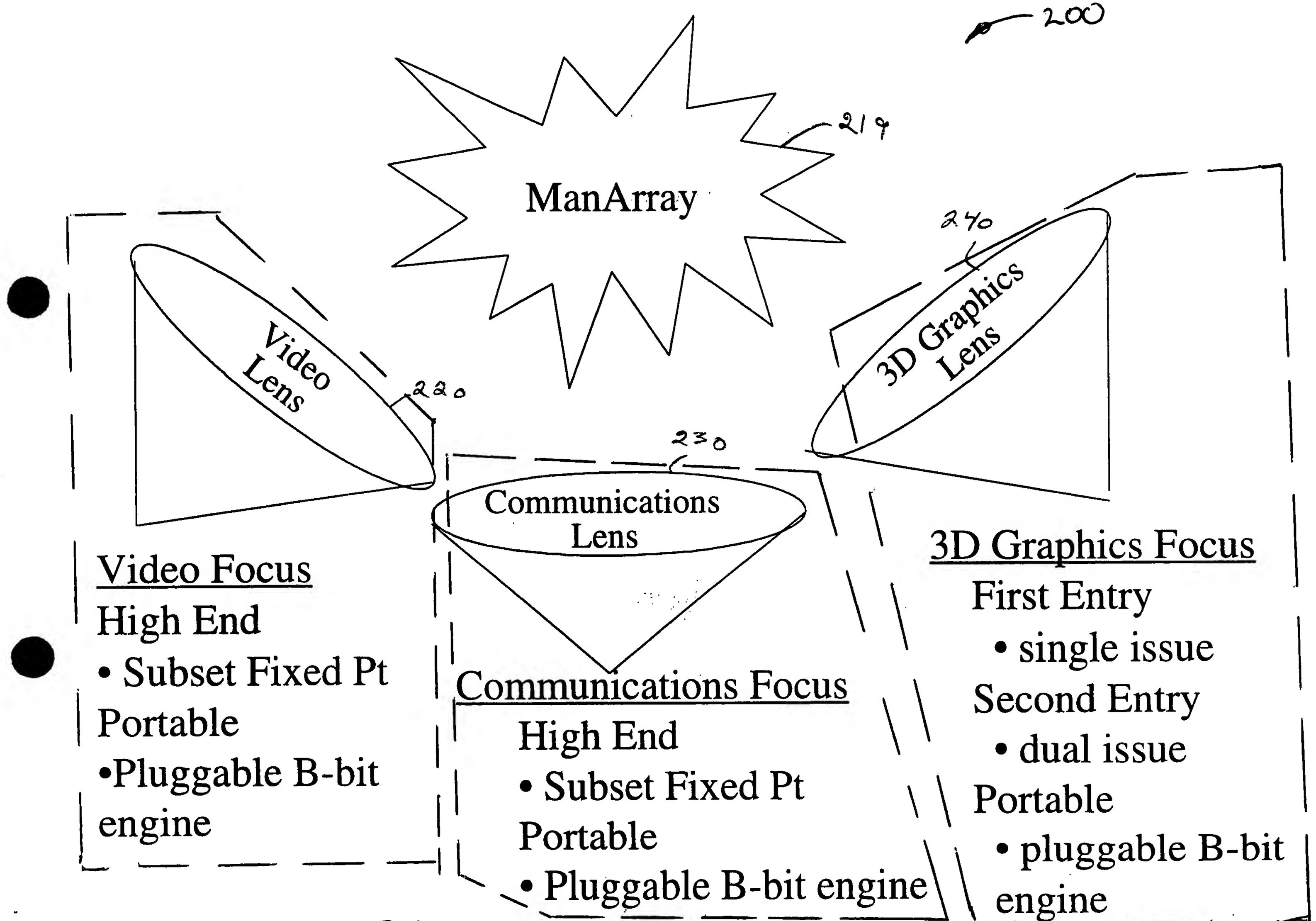
200
219
ManArray
240
Video Lens
220
230
3D Graphics Lens
Communications Lens
Video Focus
High End
• Subset Fixed Pt
Portable
•Pluggable B-bit engine
Communications Focus
High End
• Subset Fixed Pt
Portable
• Pluggable B-bit engine
3D Graphics Focus
First Entry
• single issue
Second Entry
• dual issue
Portable
• pluggable B-bit engine

FIG. 2

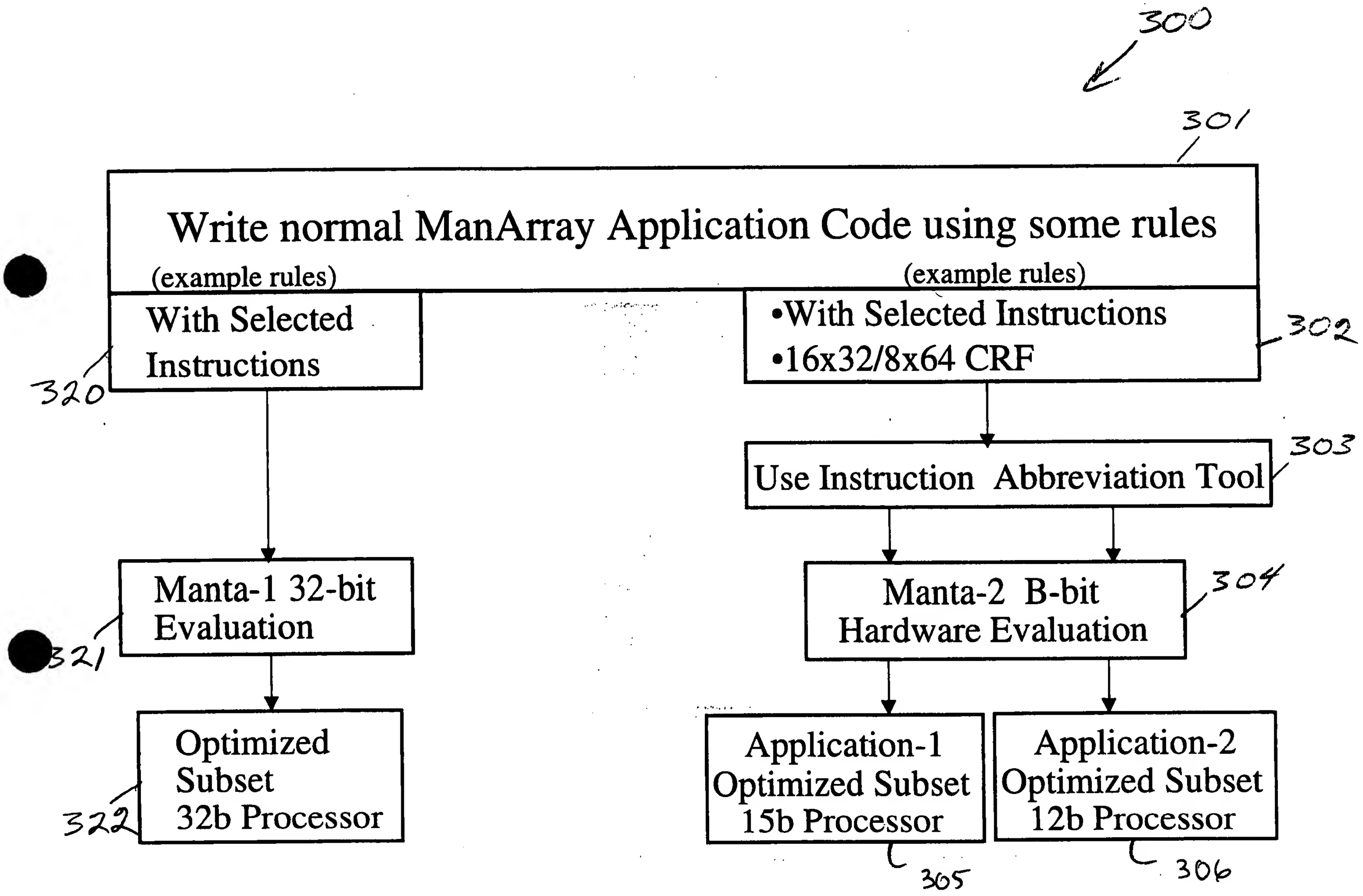
300
301
Write normal ManArray Application Code using some rules
(example rules)
With Selected Instructions
320
(example rules)
•With Selected Instructions
•16x32/8x64 CRF
302
Use Instruction Abbreviation Tool
303
Manta-1 32-bit Evaluation
321
Manta-2 B-bit Hardware Evaluation
304
Optimized Subset 32b Processor
322
Application-1 Optimized Subset 15b Processor
305
Application-2 Optimized Subset 12b Processor
306

FIG. 3A

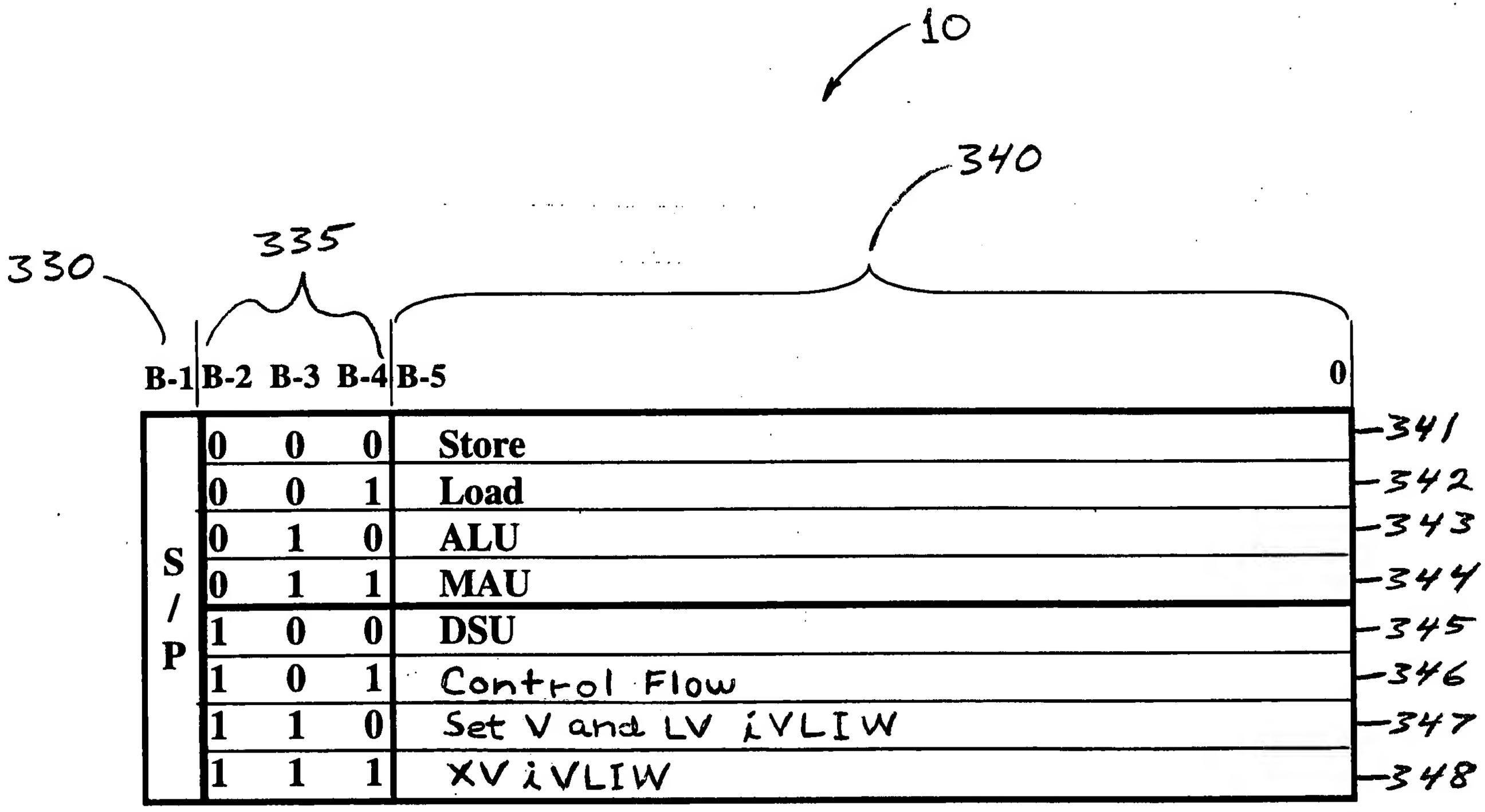

FIG. 3B

09420015 - 102100

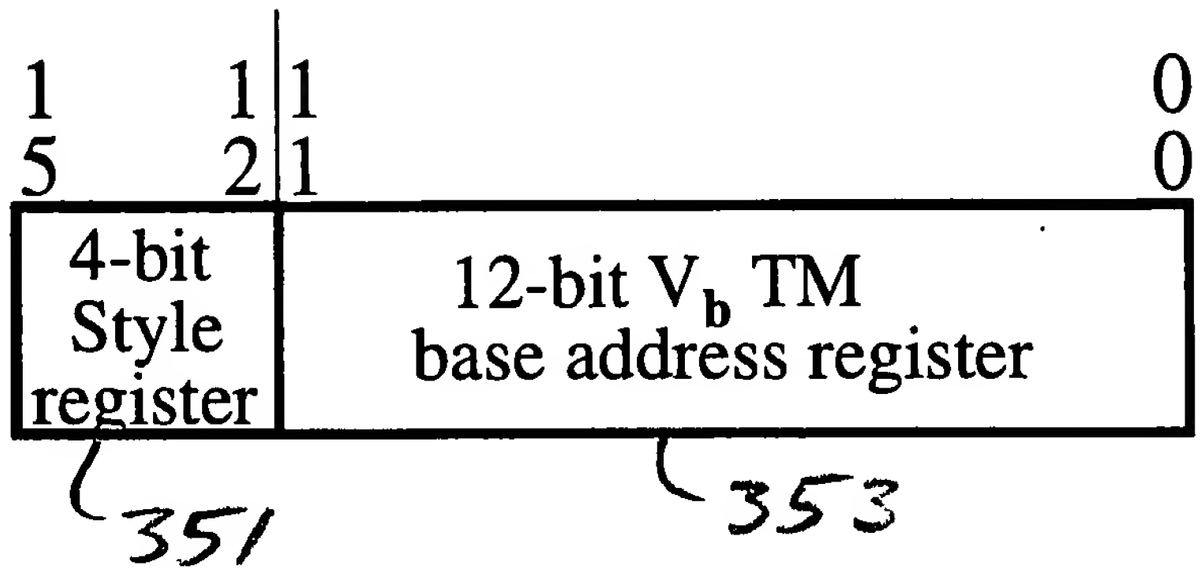
350
15
12
11
0
5
2
1
0
4-bit
Style
register
12-bit V_b TM
base address register
351
353

FIG. 3C

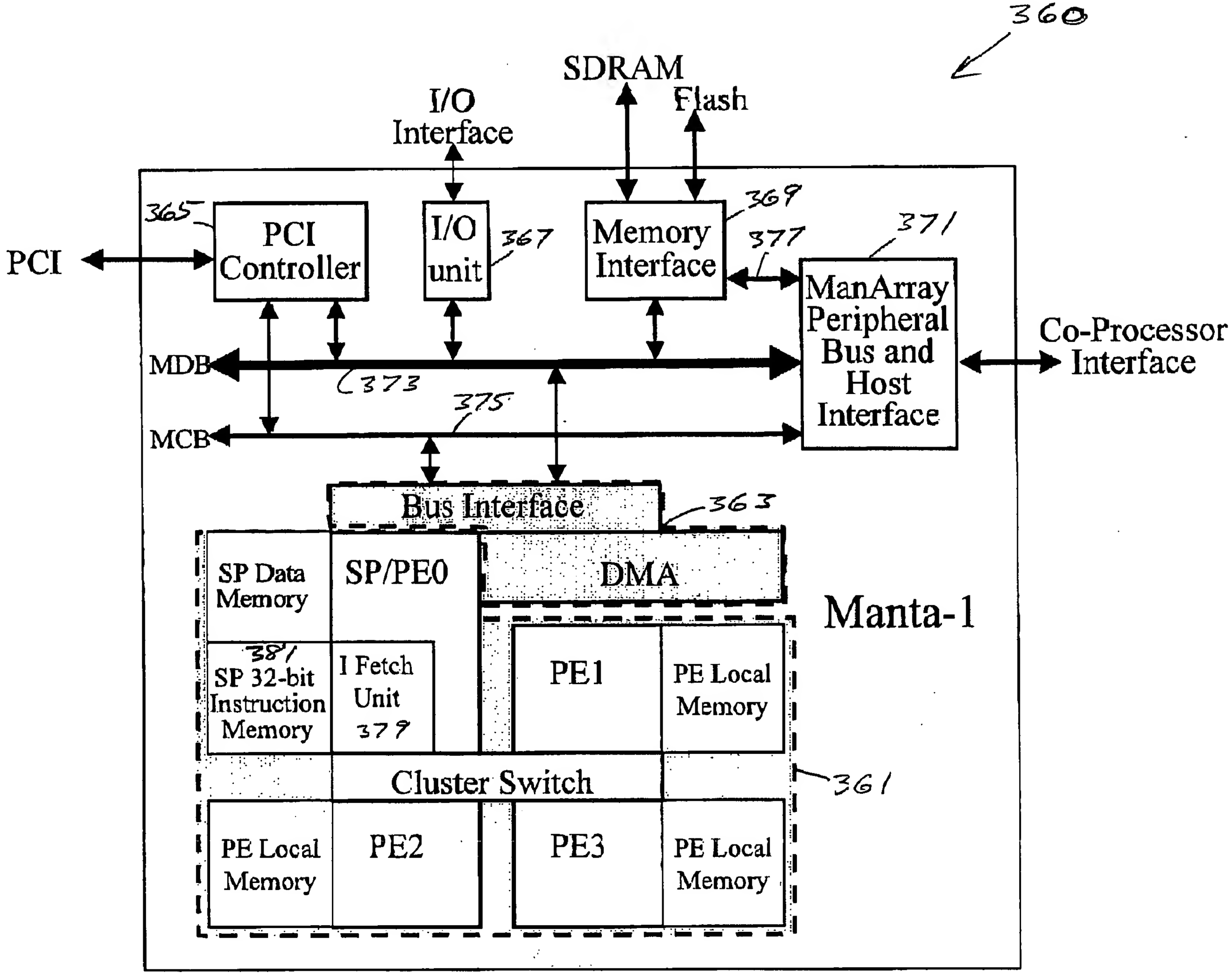
360
SDRAM
Flash
I/O
Interface
365
PCI
PCI
Controller
I/O
unit
367
Memory
Interface
369
377
371
ManArray
Peripheral
Bus and
Host
Interface
Co-Processor
Interface
MDB
373
375
MCB
Bus Interface
363
SP Data
Memory
SP/PE0
DMA
Manta-1
381
SP 32-bit
Instruction
Memory
I Fetch
Unit
379
PE1
PE Local
Memory
Cluster Switch
361
PE Local
Memory
PE2
PE3
PE Local
Memory

FIG. 3D

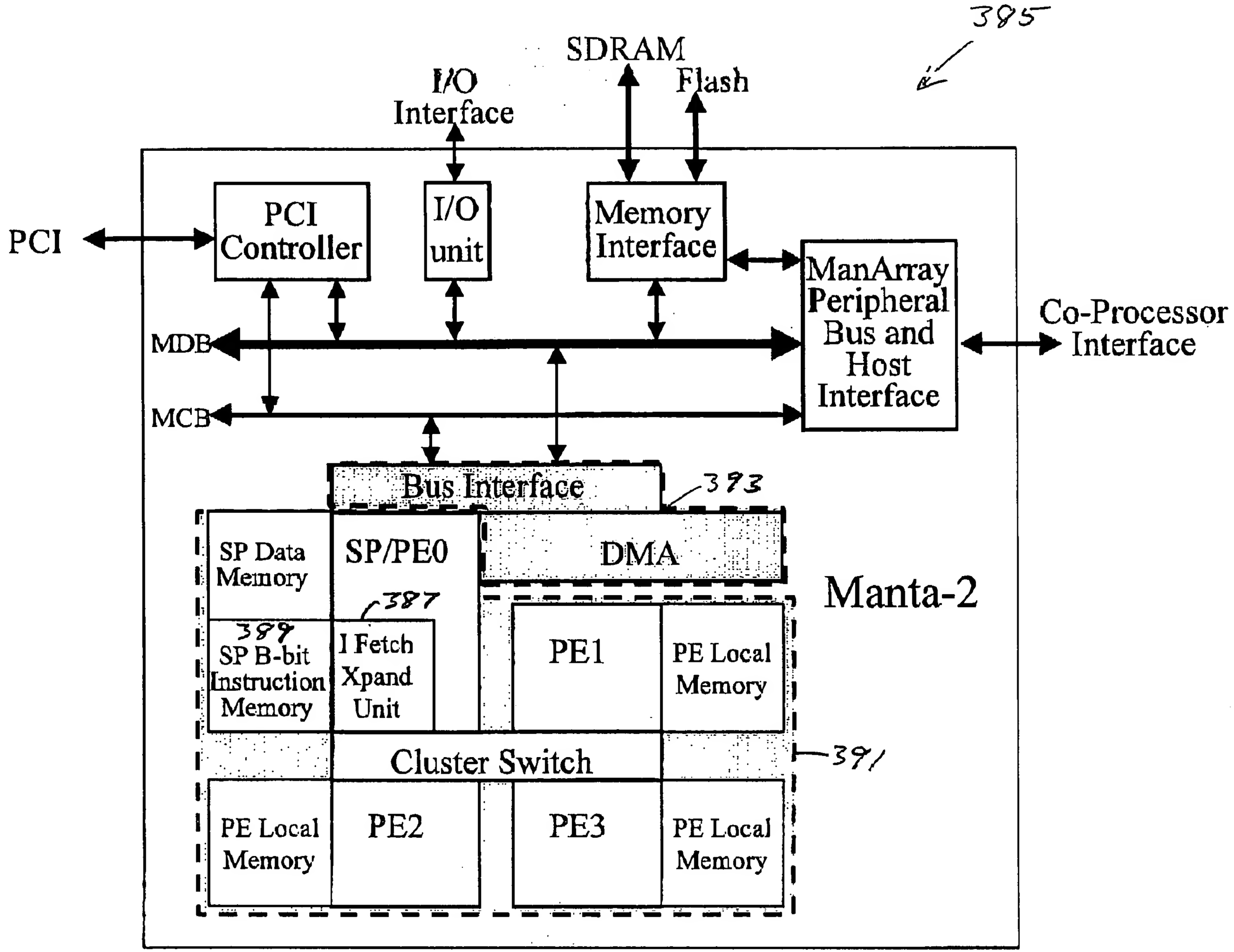
395
SDRAM
I/O Interface
Flash
PCI
PCI Controller
I/O unit
Memory Interface
ManArray Peripheral Bus and Host Interface
Co-Processor Interface
MDB
MCB
Bus Interface
393
SP Data Memory
SP/PE0
DMA
387
389
SP B-bit Instruction Memory
I Fetch Xpand Unit
PE1
PE Local Memory
Manta-2
Cluster Switch
391
PE Local Memory
PE2
PE3
PE Local Memory

FIG. 3E

SUBSTITUTE SHEET

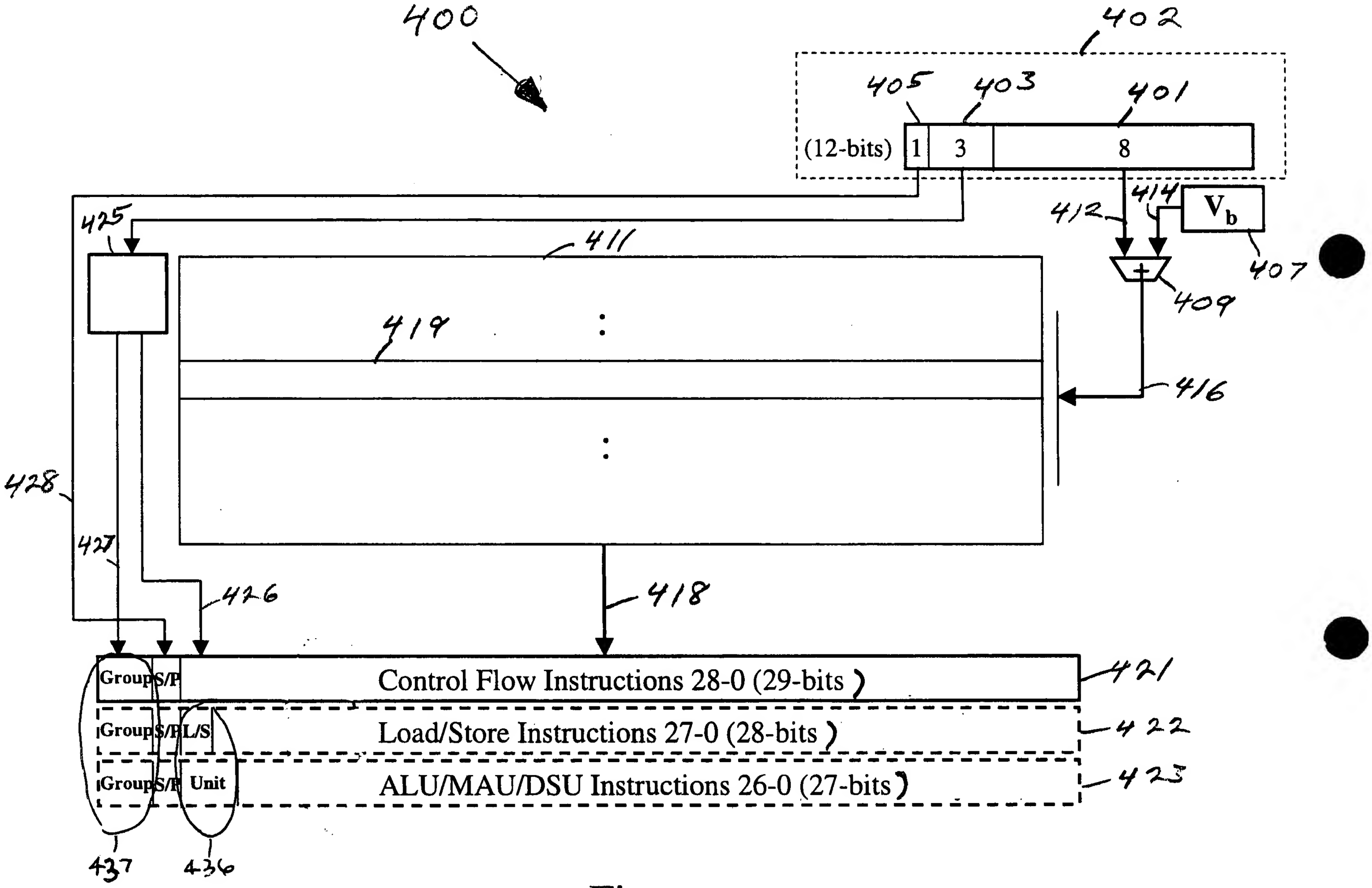

Fig. 4

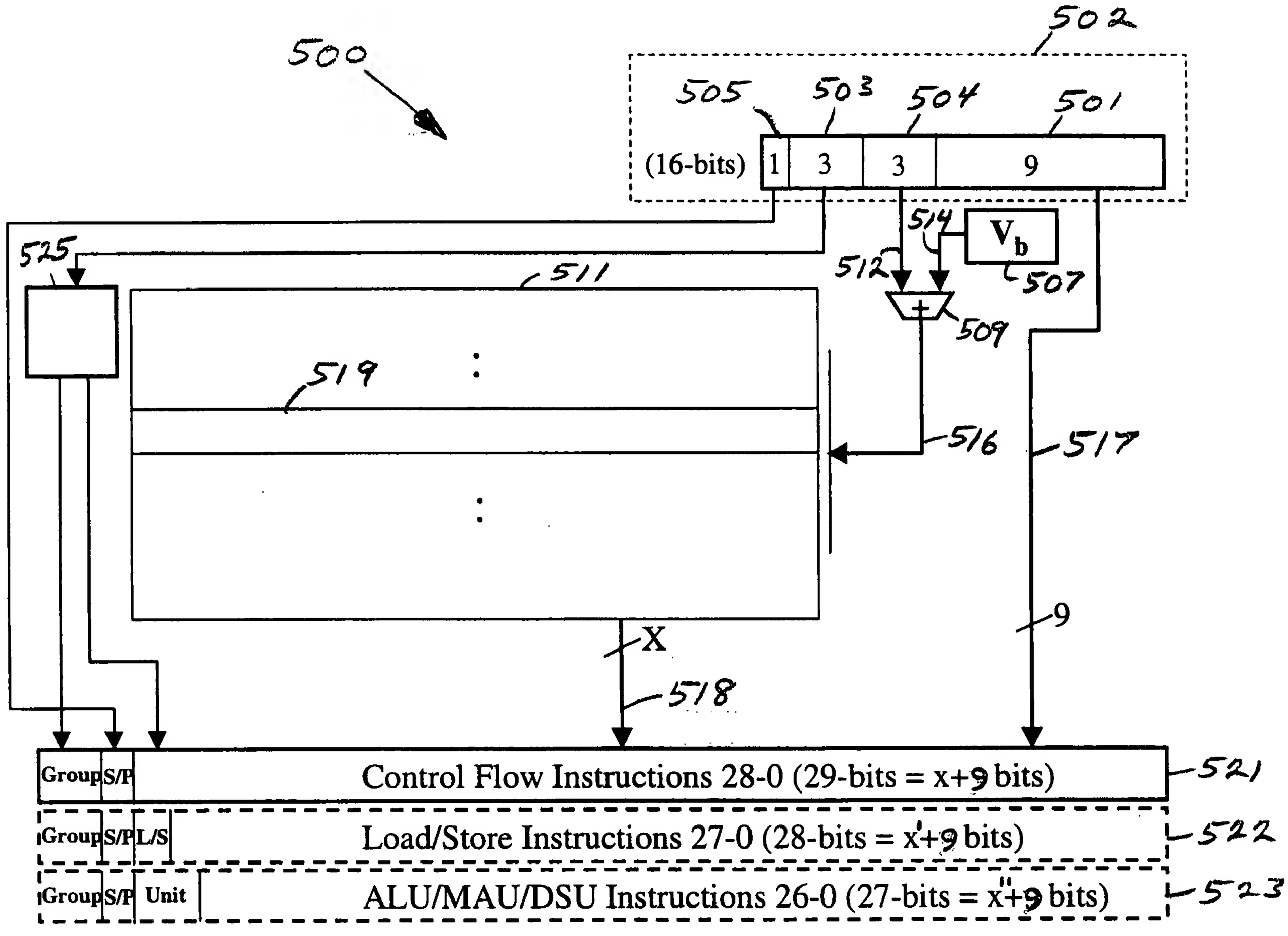
500
502
505
503
504
501
(16-bits)
1
3
3
9
514
V_b
512
507
509
525
511
519
516
517
X
9
518
Group
S/P
Control Flow Instructions 28-0 (29-bits = x+9 bits)
521
Group
S/P
L/S
Load/Store Instructions 27-0 (28-bits = x'+9 bits)
522
Group
S/P
Unit
ALU/MAU/DSU Instructions 26-0 (27-bits = x''+9 bits)
523

Fig. 5A

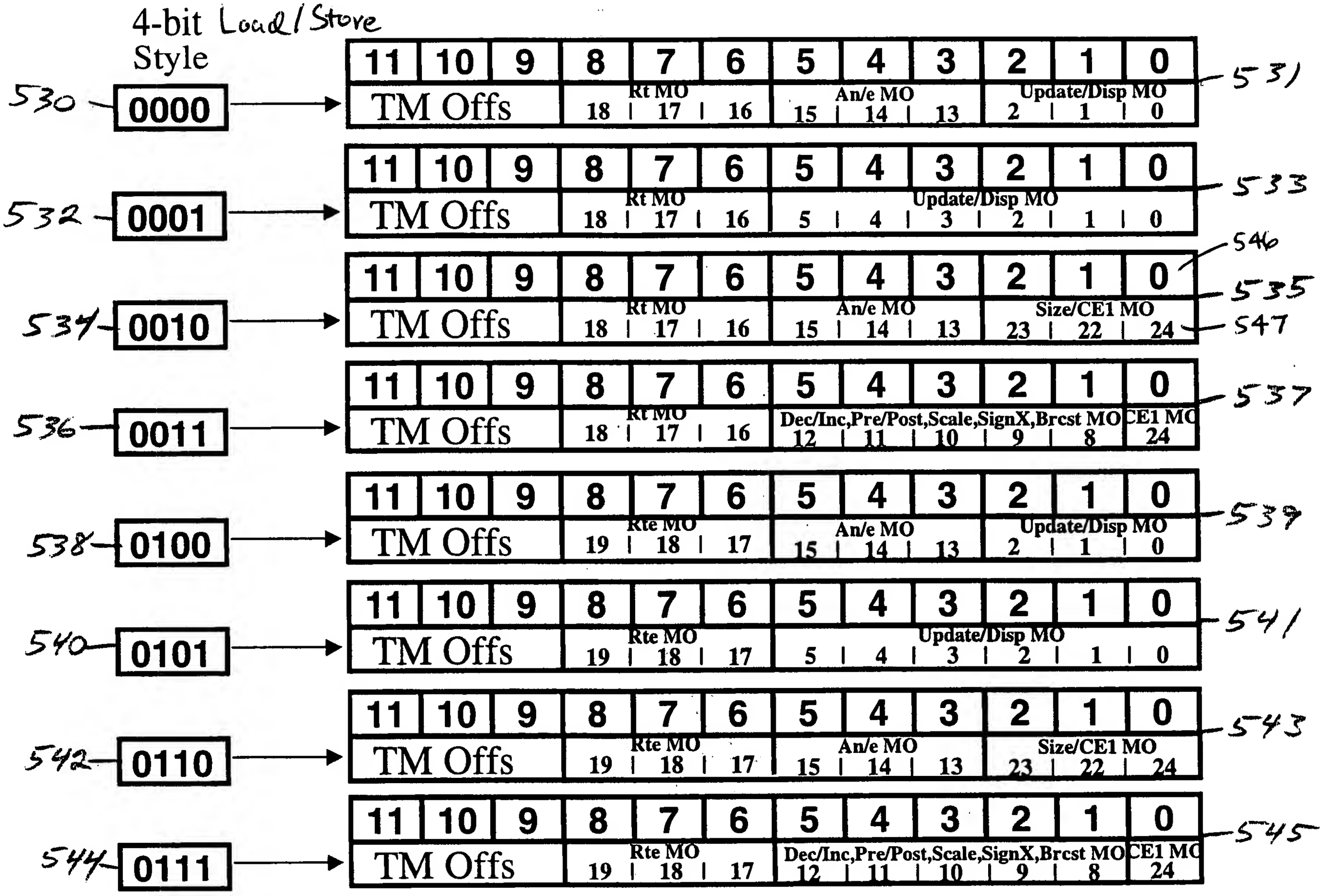
4-bit Load/Store Style
530
0000
TM Offs
11 10 9 8 7 6 5 4 3 2 1 0
Rt MO 18 17 16
An/e MO 15 14 13
Update/Disp MO 2 1 0
531
532
0001
TM Offs
Rt MO 18 17 16
Update/Disp MO 5 4 3 2 1 0
533
534
0010
TM Offs
Rt MO 18 17 16
An/e MO 15 14 13
Size/CE1 MO 23 22 24
546
535
547
536
0011
TM Offs
Rt MO 18 17 16
Dec/Inc,Pre/Post,Scale,SignX,Brcst MO 12 11 10 9 8
CE1 MO 24
537
538
0100
TM Offs
Rte MO 19 18 17
An/e MO 15 14 13
Update/Disp MO 2 1 0
539
540
0101
TM Offs
Rte MO 19 18 17
Update/Disp MO 5 4 3 2 1 0
541
542
0110
TM Offs
Rte MO 19 18 17
An/e MO 15 14 13
Size/CE1 MO 23 22 24
543
544
0111
TM Offs
Rte MO 19 18 17
Dec/Inc,Pre/Post,Scale,SignX,Brcst MO 12 11 10 9 8
CE1 MO 24
545

FIG. 5B

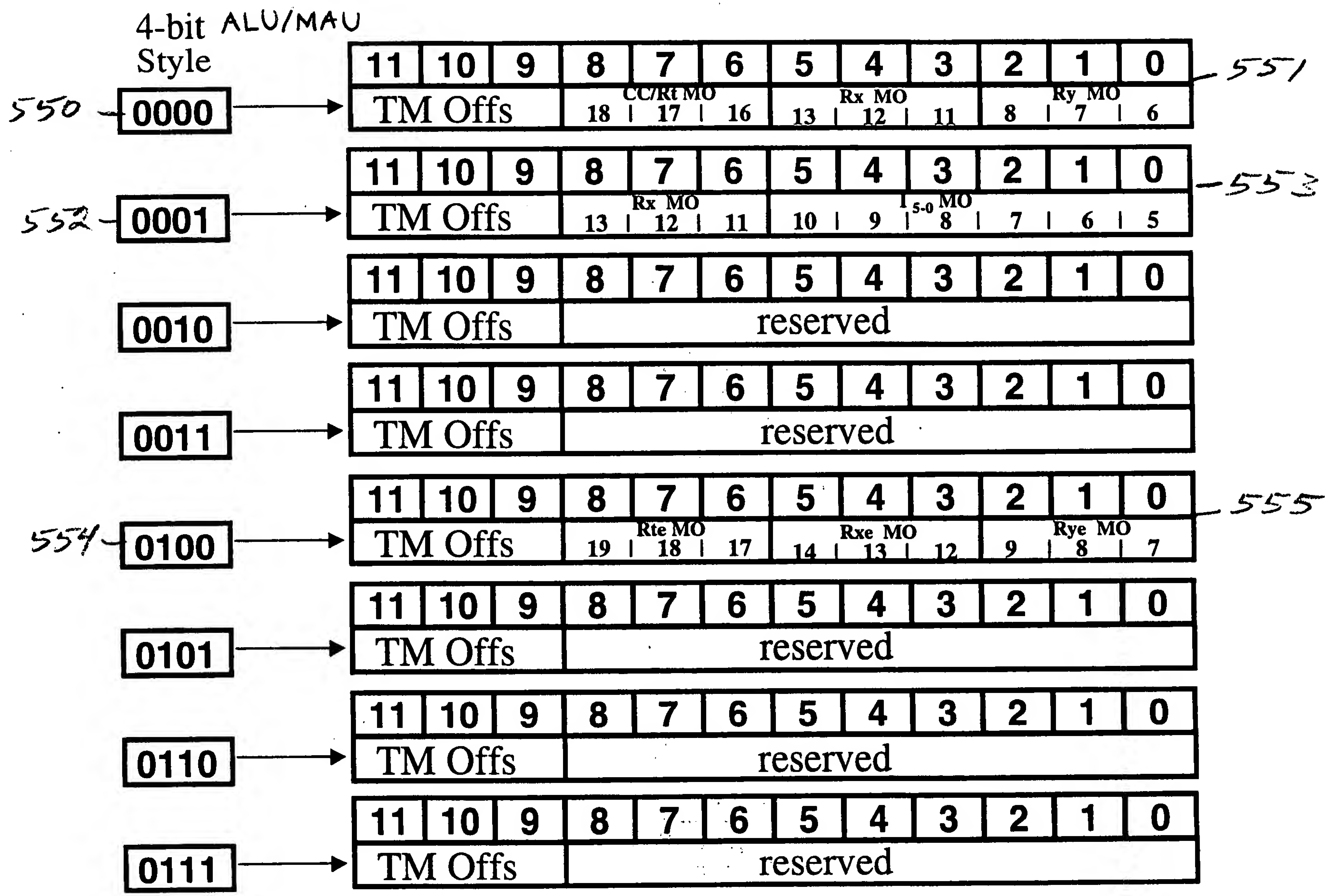
4-bit ALU/MAU Style
550
0000
TM Offs
CC/Rt MO
18 17 16
Rx MO
13 12 11
Ry MO
8 7 6
551
552
0001
TM Offs
Rx MO
13 12 11
I5-0 MO
10 9 8 7 6 5
553
0010
TM Offs
reserved
0011
TM Offs
reserved
554
0100
TM Offs
Rte MO
19 18 17
Rxe MO
14 13 12
Rye MO
9 8 7
555
0101
TM Offs
reserved
0110
TM Offs
reserved
0111
TM Offs
reserved
11 10 9 8 7 6 5 4 3 2 1 0

FIG. 5C

DETAILED DESCRIPTION

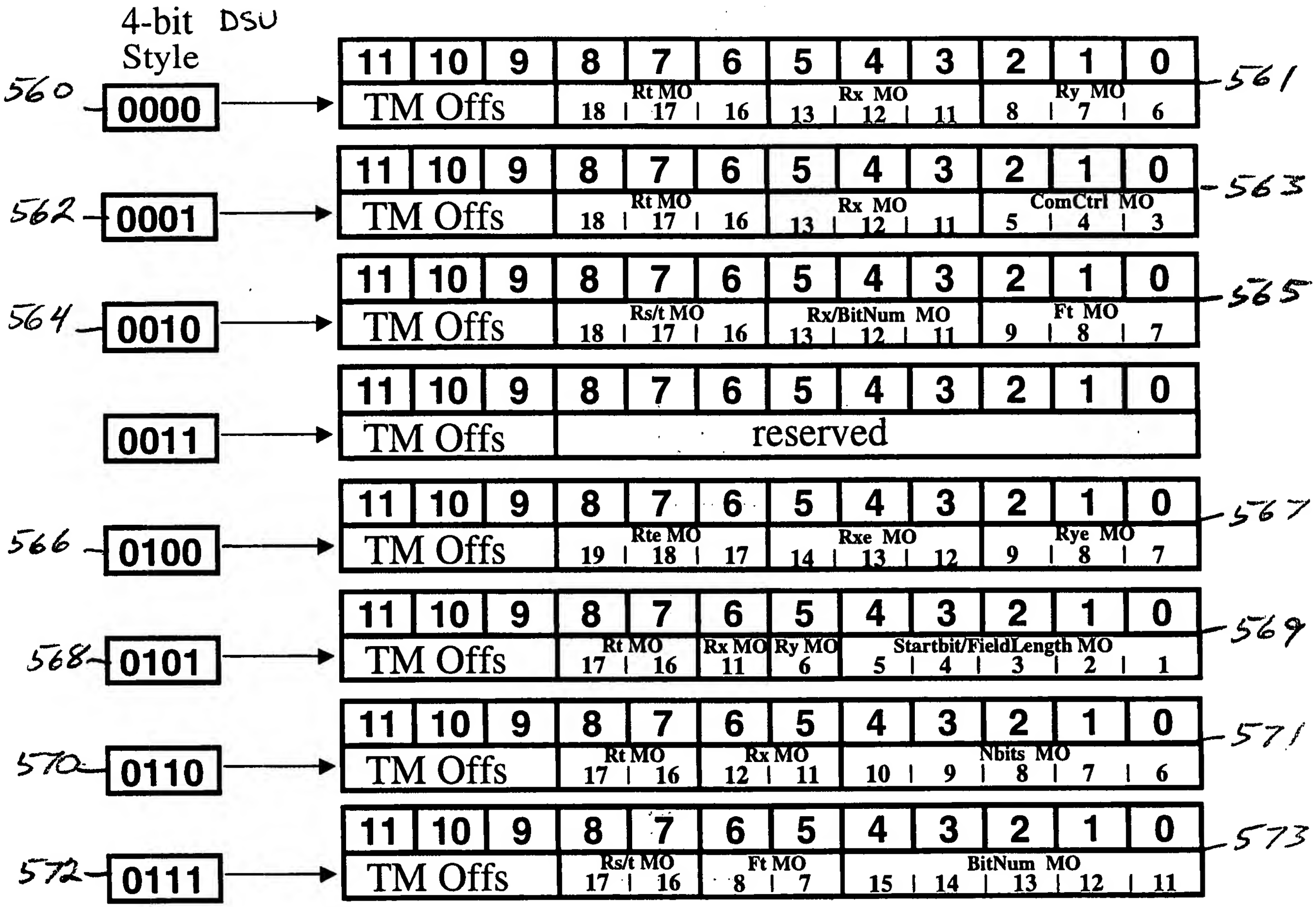

FIG. 5D

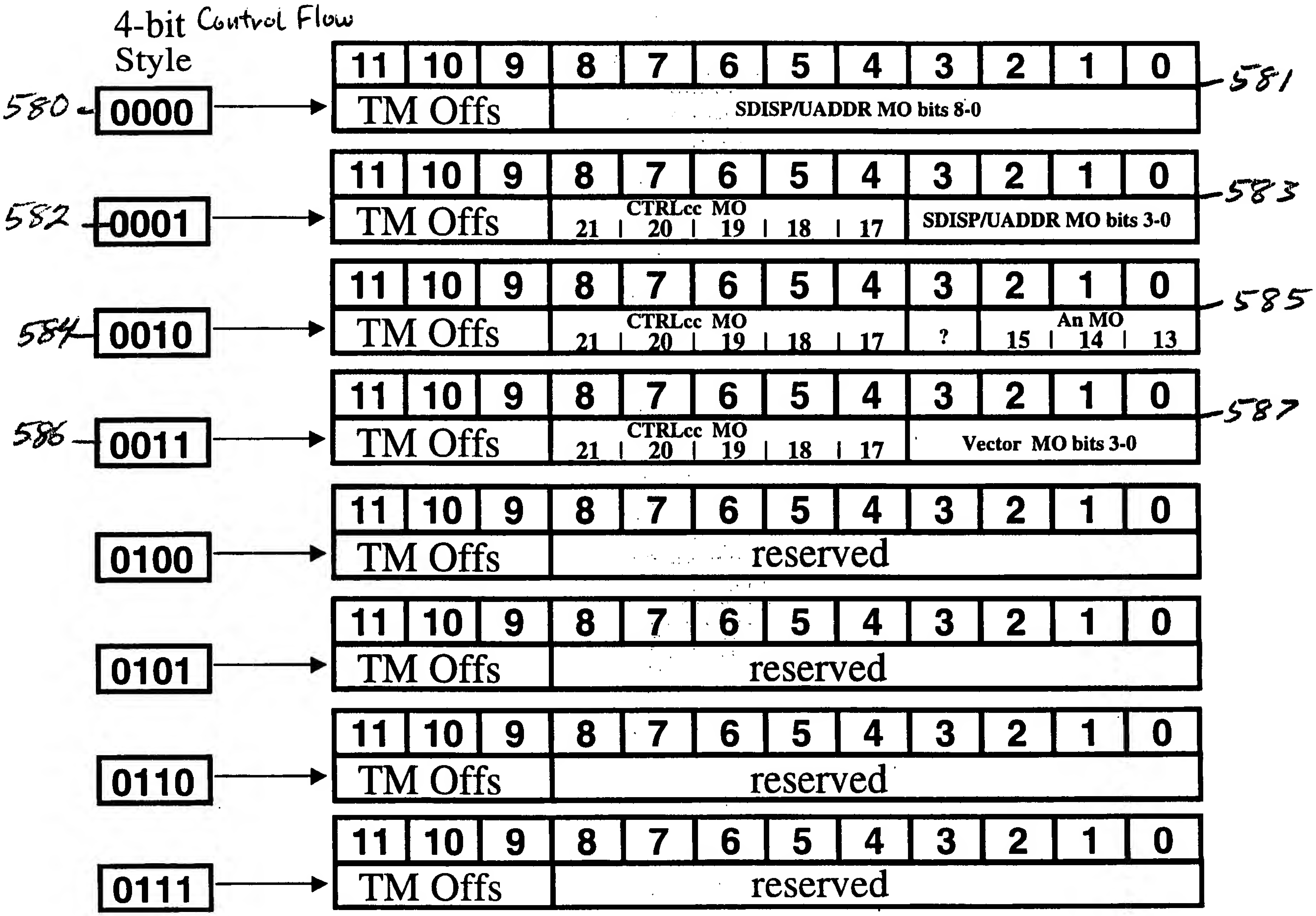
4-bit Control Flow
Style
580
0000
TM Offs
SDISP/UADDR MO bits 8-0
581
582
0001
TM Offs
CTRLcc MO
21 20 19 18 17
SDISP/UADDR MO bits 3-0
583
584
0010
TM Offs
CTRLcc MO
21 20 19 18 17
?
An MO
15 14 13
585
586
0011
TM Offs
CTRLcc MO
21 20 19 18 17
Vector MO bits 3-0
587
0100
TM Offs
reserved
0101
TM Offs
reserved
0110
TM Offs
reserved
0111
TM Offs
reserved
11 10 9 8 7 6 5 4 3 2 1 0

FIG. 5E

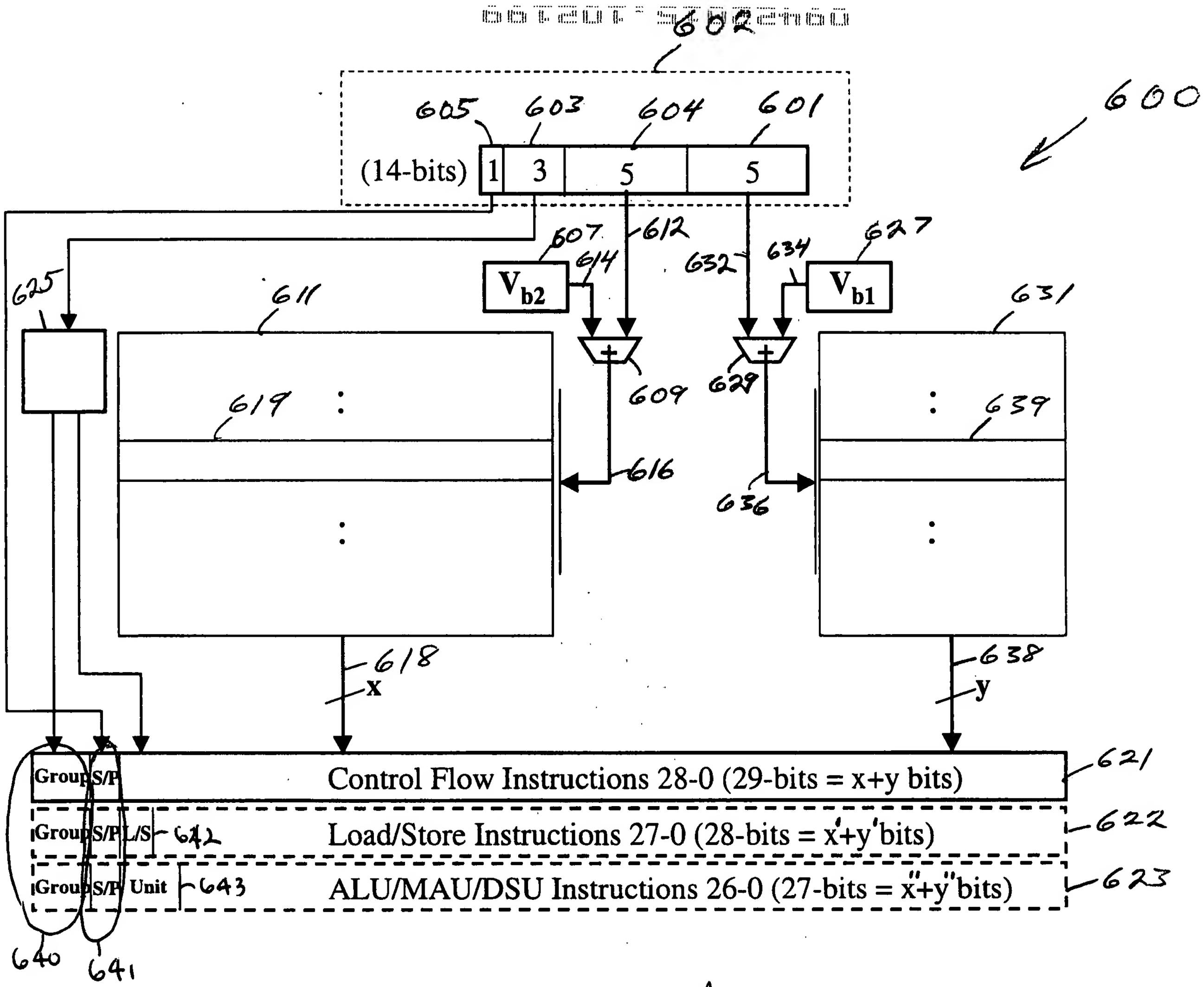
602
600
605
603
604
601
(14-bits)
1
3
5
5
607
612
614
632
634
627
625
V_{b2}
V_{b1}
611
631
609
629
619
639
616
636
618
638
x
y
621
Group S/P
Control Flow Instructions 28-0 (29-bits = x+y bits)
622
Group S/P L/S
642
Load/Store Instructions 27-0 (28-bits = x'+y'bits)
623
Group S/P Unit
643
ALU/MAU/DSU Instructions 26-0 (27-bits = x''+y''bits)
640
641

Fig. 6A

650

13	12	11	10	9	8	7	6	5	4	3	2	1	0
S / P	XV iVLIW 111			4-bit TM2Offs Vb=V0				6-bit TM1Offs Vb=V0					

652 656 654

FIG. 6B

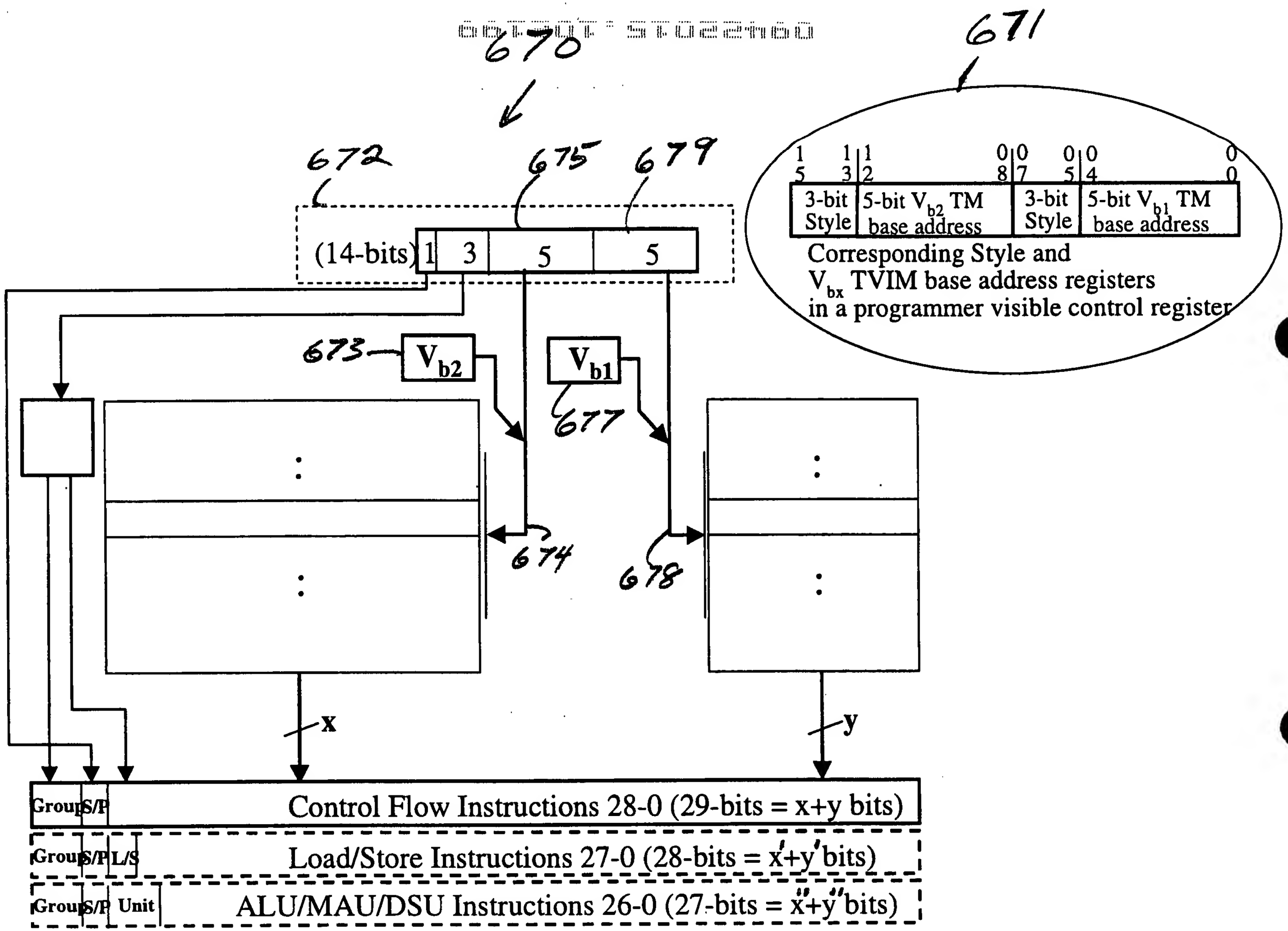
670
671
672
675
679
(14-bits)
1
3
5
5
673
V_{b2}
V_{b1}
677
674
678
x
y
Group
S/P
L/S
Unit
Control Flow Instructions 28-0 (29-bits = x+y bits)
Load/Store Instructions 27-0 (28-bits = x'+y' bits)
ALU/MAU/DSU Instructions 26-0 (27-bits = x"+y" bits)
15 13 12 8 7 5 4 0
3-bit Style
5-bit V_{b2} TM base address
3-bit Style
5-bit V_{b1} TM base address
Corresponding Style and
V_{bx} TVIM base address registers
in a programmer visible control register

Fig. 6C

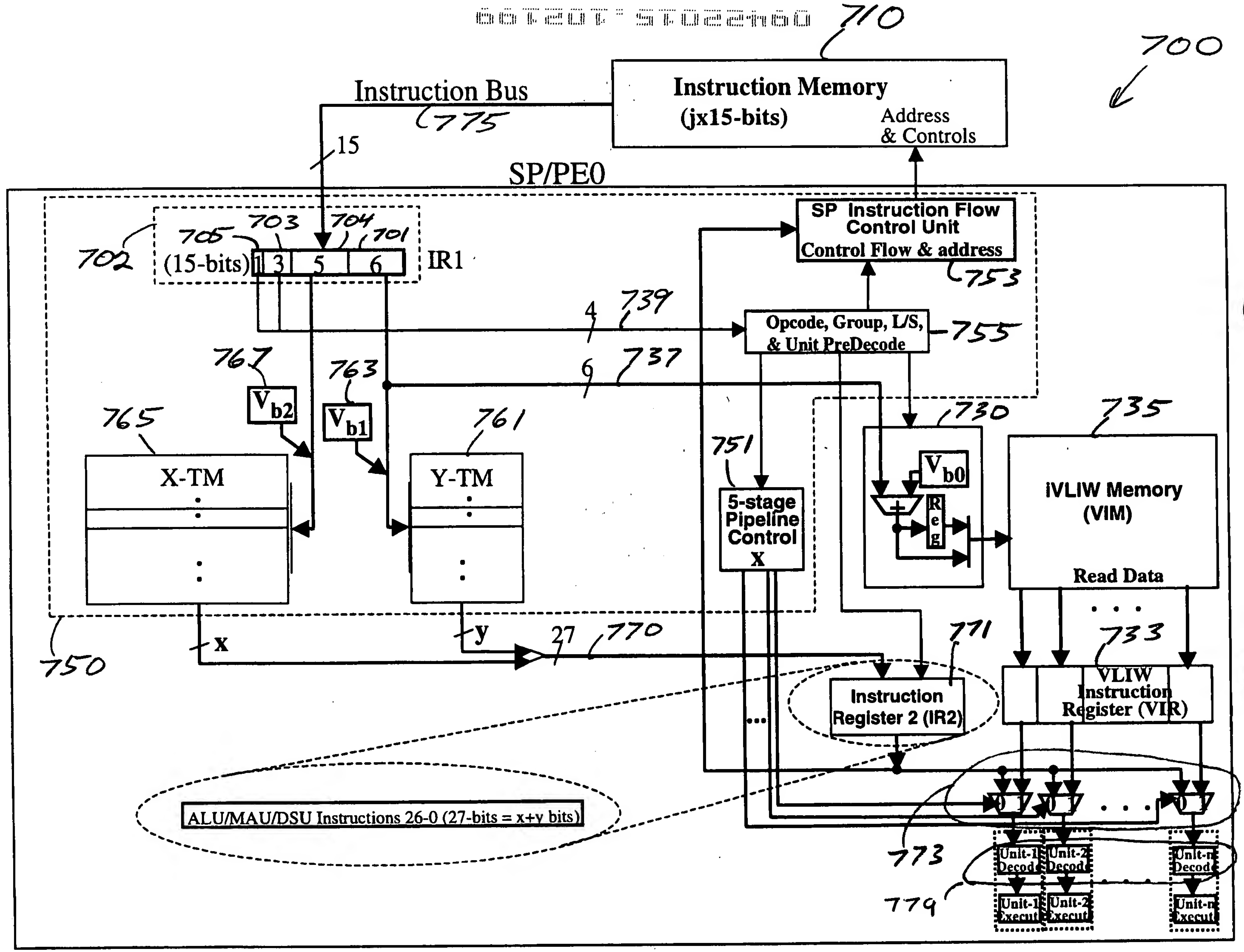
700
710
Instruction Memory
(jx15-bits)
Address
& Controls
Instruction Bus
775
15
SP/PE0
SP Instruction Flow
Control Unit
Control Flow & address
753
702
705
703
704
701
(15-bits)
1
3
5
6
IR1
4
739
Opcode, Group, L/S,
& Unit PreDecode
755
767
V_{b2}
763
V_{b1}
6
737
730
V_{b0}
Reg
735
765
X-TM
761
Y-TM
751
5-stage
Pipeline
Control
X
iVLIW Memory
(VIM)
Read Data
733
750
x
y
27
770
771
Instruction
Register 2 (IR2)
VLIW
Instruction
Register (VIR)
ALU/MAU/DSU Instructions 26-0 (27-bits = x+y bits)
773
779
Unit-1 Decode
Unit-2 Decode
Unit-n Decode
Unit-1 Execute
Unit-2 Execute
Unit-n Execute

FIG. 7

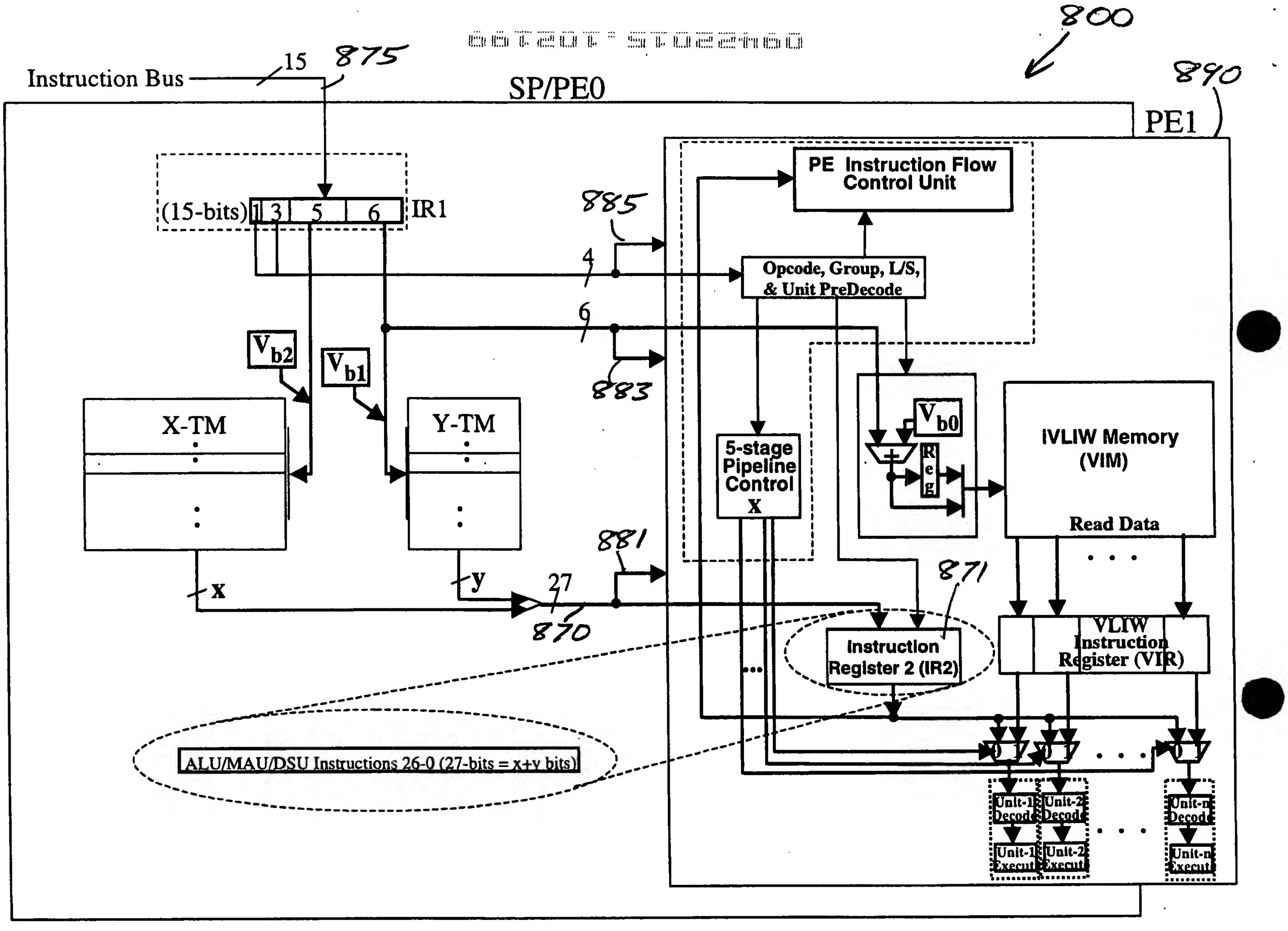
800
875
15
Instruction Bus
SP/PE0
890
PE1
(15-bits) 1 3 5 6 IR1
885
4
6
883
PE Instruction Flow Control Unit
Opcode, Group, L/S, & Unit PreDecode
V_{b2}
V_{b1}
V_{b0}
X-TM
Y-TM
5-stage Pipeline Control X
IVLIW Memory (VIM)
Read Data
881
871
x
y
27
870
Instruction Register 2 (IR2)
VLIW Instruction Register (VIR)
ALU/MAU/DSU Instructions 26-0 (27-bits = x+y bits)
Unit-1 Decode
Unit-2 Decode
Unit-n Decode
Unit-1 Execute
Unit-2 Execute
Unit-n Execute

FIG. 8

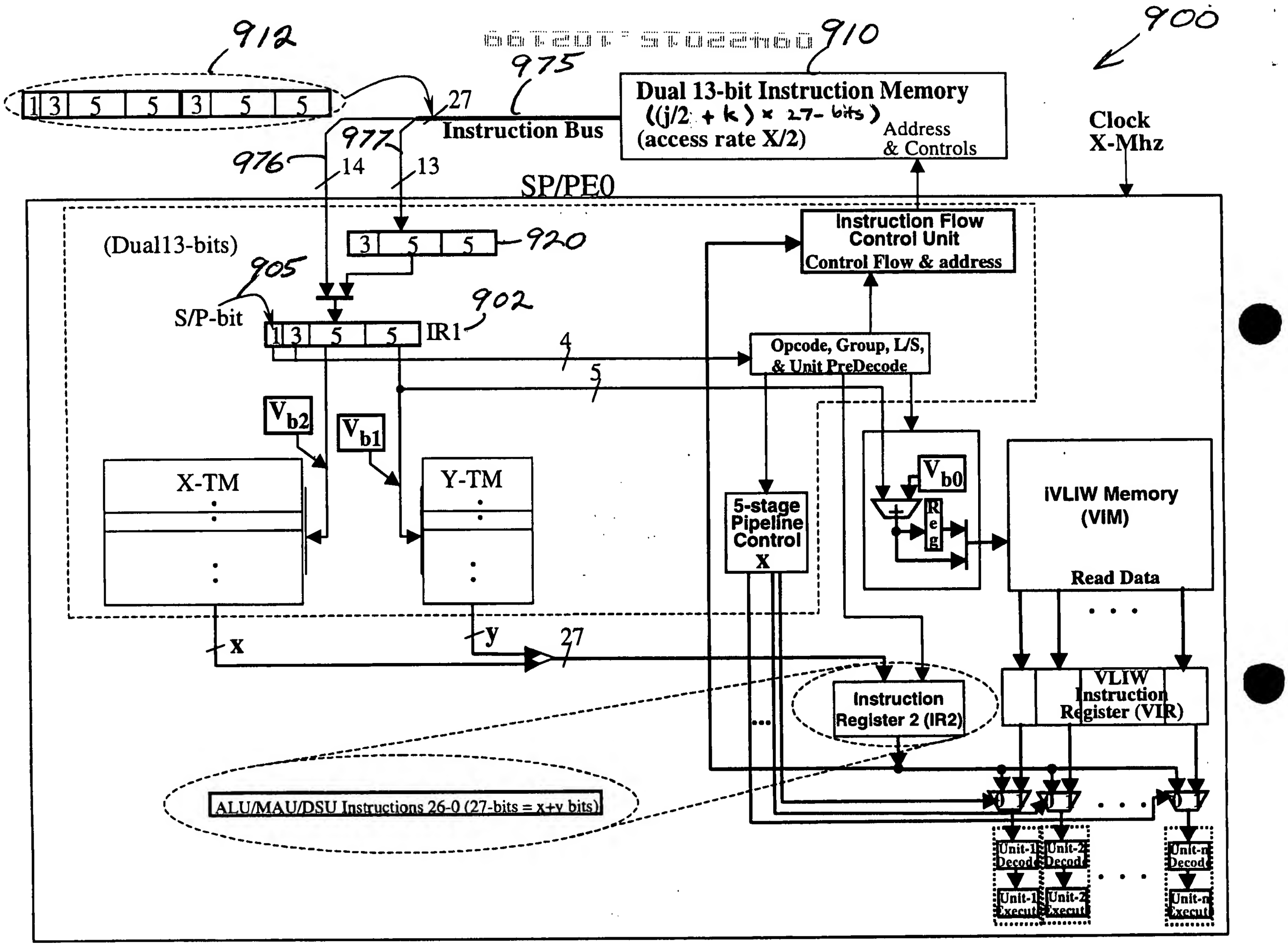
912
910
900
975
1 3 5 5 3 5 5
27
Instruction Bus
Dual 13-bit Instruction Memory
((j/2 + k) × 27- bits)
(access rate X/2)
Address
& Controls
Clock
X-Mhz
977
976
14
13
SP/PE0
(Dual13-bits)
3 5 5
920
905
S/P-bit
902
1 3 5 5
IR1
Instruction Flow
Control Unit
Control Flow & address
4
5
Opcode, Group, L/S,
& Unit PreDecode
Vb2
Vb1
Vb0
X-TM
Y-TM
5-stage
Pipeline
Control
x
Reg
IVLIW Memory
(VIM)
Read Data
x
y
27
Instruction
Register 2 (IR2)
VLIW
Instruction
Register (VIR)
ALU/MAU/DSU Instructions 26-0 (27-bits = x+y bits)
Unit-1
Decode
Unit-2
Decode
Unit-n
Decode
Unit-1
Execute
Unit-2
Execute
Unit-n
Execute

FIG. 9

Select Standard

1000

Cycle (1015)	Fetch (1025)	Xpand & Dispatch (1035)	Decode (1045)	Execute (1055)	Cond. Ret (1065)
i (1010)	SP Fetches a B-bit Instr(i)= ADD.S Instruction & loads it into IR1	Previous Instruction Instr(i-1)	Previous Instruction Instr(i-2)	Previous Instruction Instr(i-3)	Previous Instruction Instr(i-4)
i+1 (1020)	SP Fetches a B-bit Instr(i+1)=XV.S instruction & loads it into IR1	S/P-bit indicates an SP only operation. Local TM fetches occur and a native form of the Instr(i)=ADD.S instruction is loaded into IR2. The S/P-bit and 3-bit opcode are decoded in the SP.	Previous Instruction Instr(i-1)	Previous Instruction Instr(i-2)	Previous Instruction Instr(i-3)
i+2 (1030)	SP Fetches a B-bit Instr(i+2)=COPY.S instruction & loads it into IR1	S/P-bit & opcode indicate an SP XV operation. Local TM fetches occur and a native form of the Instr(i+1)=XV.S Instruction is loaded into IR2. The S/P-bit, and 3-bit opcode are decoded in the SP. TheVIM address is calculated and the iVLIW is fetched from the XV VIM	The ALU decodes Instr(i)=ADD.S Instruction	Previous Instruction Instr(i-1)	Previous Instruction Instr(i-2)
i+3 (1040)	SP Fetches a B-bit Instr(i+3)=ADD.S instruction & loads it into IR1	S/P-bit indicates an SP only operation. Local TM fetches occur and a native form of the Instr(i+2)=COPY.S Instruction is loaded into IR2.	Instr(i+1)=XV.S causes up to 5 Instructions in iVLIW decode	The ALU executes Instr(i)=ADD.S Instruction.	Previous Instruction Instr(i-1)
i+4 (1050)	Fetch next B-bit instruction: Instr(i+4)	S/P-bit indicates an SP only operation. Local TM fetches occur and a native form of the Instr(i+3)=ADD.S Instruction is loaded into IR2.	The DSU decodes the Instr(i+2)=COPY.S Instruction	Instr(i+1)=XV.S causes up to 5 Instructions in iVLIW execute	The Instr(i)=ADD.S side effects are set in ASFs and ACFs

FIG. 10